A Highly-Integrated Low-Power Direct Conversion Receiver MMIC for Broadband Wireless Applications

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***Abstract* — In this paper, we present a highly integrated low-power direct conversion receiver MMIC for broadband wireless applications at C-band. This receiver chip is fabricated in a 0.6 μm commercial GaAs MESFET process and operates on only 90 mW of dc power consumption. Using an integrated switched LNA and direct-coupled baseband amplifiers, this receiver demonstrates a conversion gain of 25 dB, NF of 6.7 dB, dc offset below –70 dBm, IIP2 of +20 dBm, and IIP3 of -15 dBm in the high-gain mode and +15 dBm in the low-gain mode at 5.8 GHz.**

I. Introduction

With the growing interest in the broadband applications at C-band frequencies, the need for highly integrated low-power solutions is rapidly increasing. This has placed a great demand on receiver topologies such as direct conversion that can be implemented in a compact and cost-effective manner.

In a direct conversion receiver there is no concern for the image frequencies and channel selection can be simplified to active low pass filtering at the baseband. However, several challenging design issues appear in direct conversion topology that require special attention to the mixer design and frequency scheme of these receivers. The most important of these design issues are even-order intermodulations, LO radiation, dc offsets and dc power consumption. A variety of direct conversion receivers have been implemented in both GaAs and Si, but these receivers mostly present a compromise between linearity, dc offsets, dc power consumption, and level of on-chip integration [1-5].

Using a commercial GaAs Metal-Semiconductor FET (MESFET), we previously demonstrated the first compact C-band direct conversion receiver, which addressed the majority of the needed specifications [6]. In this paper, we introduce a new low-power MMIC that incorporates a switched low-noise amplifier (LNA) and direct coupled baseband amplifiers to significantly improve noise figure and conversion gain while maintaining the required linearity and dc-offset performance. This receiver MMIC consumes only 90 mW of dc power from a 3 volt supply and occupies 75x60 mil^2 of die area.

II. Block Design

The block diagram of this receiver is shown in Fig.1. This receiver is composed of a high-linearity switched LNA followed by a Wilkinson power divider, two even-harmonic mixers, and direct-coupled baseband amplifiers. The LO is supplied to the mixers by a modified Wilkinson power divider that incorporates a 45˚ phase shift in one of the LO paths. Because of the doubling action in the mixers, only 45˚ of phase-shift is required to produce in-phase (I) and quadrature-phase (Q) signals at the mixer outputs.

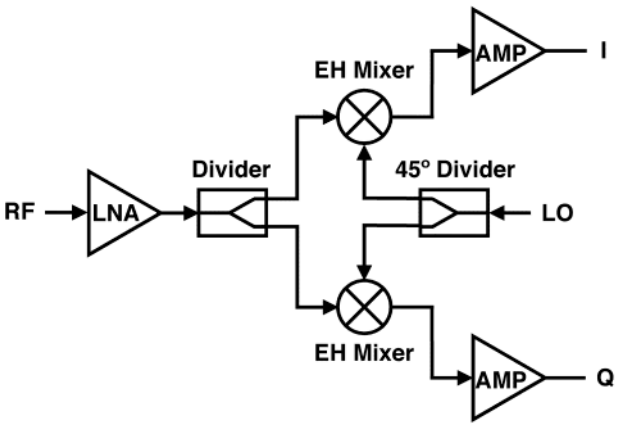


Fig. 1. Block diagram of the receiver MMIC.

A. Switched LNA

As shown in Fig. 2, this switched LNA is composed of a two-stage LNA in parallel with a bypass switch. In the

high-gain mode the LNA is turned on, and the switch is turned off to reduce feedback. This mode of operation provides the gain and NF required for good receiver sensitivity. In the low-gain mode the switch is fully turned on, and the LNA is turned off to avoid the generation of intermodulations. In this mode of operation the linearity of the LNA is improved to increase the dynamic range.

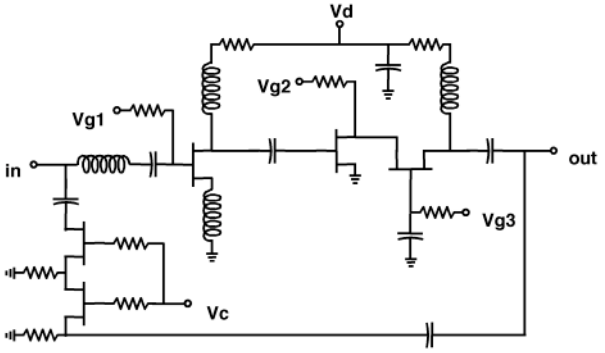


Fig. 2. Circuit schematic of the switched-LNA.

The stand-alone LNA is composed of a 400-μm common source FET followed by two 300-μm FETs in a cascode configuration [7]. This LNA has a gain of 24 dB, IIP3 of –12 dBm, and NF of 2.3 dB with 6 mA of dc current. The switch is composed of two FETs in series configuration and provides an IIP3 of +15 dBm, and loss of 8 dB with negligible dc current. Two FETs were used in the switch to increase the reverse isolation. The gain of the switched LNA is reduced in the high-gain mode because of the capacitive feedback of the switch. The overall performance of the switched LNA, which is the parallel combination of the LNA and switch, is shown in Table I. Only enhancement-mode FETs were used in the switched LNA to simplify biasing by positive supply voltages.

TABLE I
SWICTHED-LNA CHARACTERISTICS

	High-Gain Mode	Low-Gain Mode
Gain	14 dB	-8 dB
NF	2.4 dB	15 dB
IIP3	-5 dBm	+15 dBm
Current	6 mA	<1 mA
S11	-10 dB	-12 dB
S22	-13 dB	-15 dB

B. Subharmonic Mixers

Each mixer is composed of a pair of 150-μm Schottky-barrier diodes in antiparallel diode pair (APDP) configuration, interconnected with resonant tanks that are used for port to port isolation. We have previously reported the impact of diode mismatch on dc-offset performance of such APDP mixers [8]; therefore, inter-digitated APDP structures are used to improve matching and reduce such unwanted effects. Resonant tanks are made up of metal-insulator-metal (MIM) capacitors connected in parallel with spiral inductors. One resonant tank is used to isolate both the RF and IF ports from the LO signal, while the other two are used to isolate the IF port from both the RF and LO signals. By using APDP mixers we are able to increase IIP2, alleviate in-band LO leakage and reduce the time-variant dc offset [6,8]. Because of the frequency scheme of such a mixer a LO frequency of 2.9 GHz is used to down-convert the RF band of interest at 5.9 GHz. The mixers show a loss of 7 dB, IIP3 of +12 dBm, and IIP2 of above +35 dBm. Figure 3 shows the circuit schematic of the subharmonic mixers.

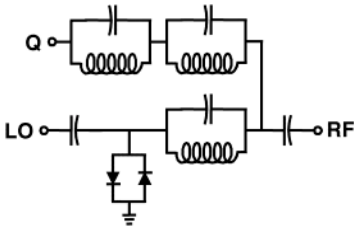


Fig. 3. Circuit schematic of the subharmonic mixer.

C. Direct-Coupled Baseband Amplifiers

Each mixer is followed by a direct-coupled baseband amplifier with a gain of 25 dB and IIP3 of -14 dBm. As shown in Fig. 4, amplifiers are composed of four common-source stages connected by level shifting diodes.

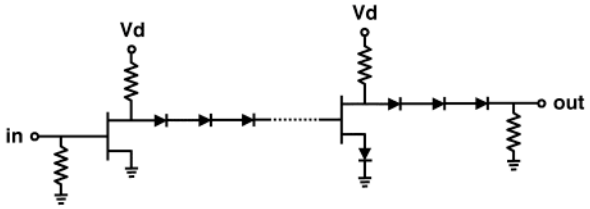


Fig. 4. Circuit schematic of the direct-coupled baseband amplifiers.

A depletion-mode FET is used for the first stage, and three enhancement-mode MESFETs make up the last three stages. By using large level shifting diodes between each stage, a large junction capacitance is created under a forward bias. This pulls the corner frequency of the amplifiers down to dc, while still rejecting the dc offsets generated in the mixers. Each amplifier consumes 12 mA of dc current and has a 3-dB bandwidth greater than 200 MHz.

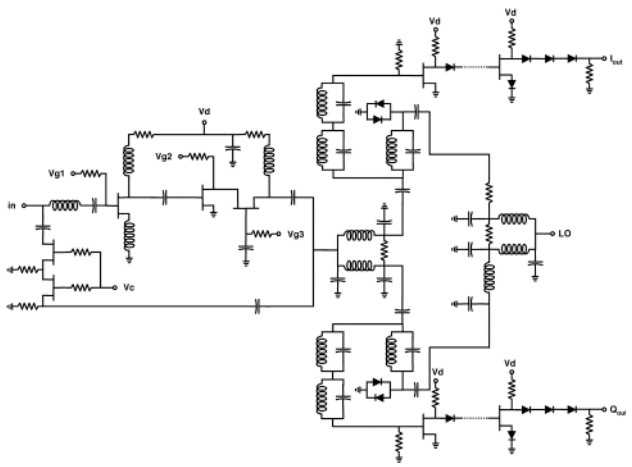
III. Integrated Receiver

All receiver blocks are integrated together on a 75x60 mil^2 die area. The overall performance of the receiver is shown in Table II. The receiver demonstrates excellent IIP3 in the low-gain mode and sufficiently high IIP3 for the high-gain operation.

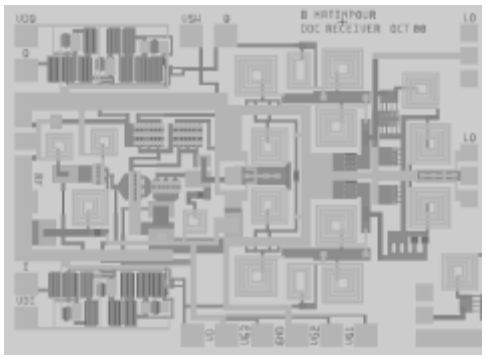
TABLE II
RECEIVER CHARACTERISTICS

	High-Gain Mode	Low-Gain Mode
Gain	25 dB	-8 dB
NF	6.7 dB	20 dB
Dc offset	-70 dBm	-71 dBm
IIP3	-15 dBm	+6 dBm
IIP2	20 dBm	22 dBm
Current	30 mA	24 mA
S11	-10 dB	-11 dB
Baseband BW	120 MHz	120 MHz

Figure 5 shows the schematic and a picture of the complete receiver in TriQuint's GaAs MESFET process.



(a)



(b)

Fig. 4. (a) Circuit schematic and (b) picture of the receiver MMIC.

IV. Conclusion

A highly integrated low-power direct conversion receiver MMIC has been demonstrated in a commercial GaAs MESFET process. A switched LNA and even-harmonic mixers are utilized to obtain excellent linearity, NF, and conversion gain. Diode matching in the mixers and direct-coupled baseband amplifiers are used to reduce the dc offset while increasing the conversion gain. This receiver demonstrates a conversion gain of 25 dB, NF of 6.7 dB, and IIP3 of -15 dBm in the high-gain mode and +15 dBm in the low-gain mode at 5.8 GHz.

Acknowledgement

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